PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Atoji et al	)	Examiner:
Serial No.: To be assigned	)	Art Unit:
Filed: Herewith	)	
For: **BUCKETS OF COMMANDS IN A MULTIPROCESSOR-BASED VERIFICATION ENVIRONMENT**	)	

Docket No.: RPS920010172US1 (IRA-10-5709)

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

This Information Disclosure Statement is being filed to fulfill the duty of candor and good faith toward the Patent and Trademark Office, as required pursuant to 37 C.F.R. § 1.56.

Listed on the attached PTO form 1449 is information known to persons substantively involved in the preparation of the application identified above, and that a reasonable Examiner would consider important when deciding whether to allow the application. This document is not to be construed as a representation that a search to locate the most relevant information has been made, nor a representation that more pertinent information does not exist.

Copies of the information listed on the attached PTO Form 1449 are provided herewith.

The identification of any information herein is not intended to be, and should not be understood as being, an admission that such information, in fact, constitutes "prior art" within the meaning of applicable law. The "prior art" status of any information is a matter to be resolved during prosecution.

This Information Disclosure Statement is being filed concurrently with the application and, consequently, prior to an Office Action. Accordingly, it is not believed that any fee is required relating to the filing of this Information Disclosure Statement. If this is not the case, the Patent Office is hereby authorized to charge any related fee to Deposit Account No. 09-1990.

Respectfully submitted,

Date: June 2, 2003

By: _____

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Attachments

Subst. Form PTO-1449 APPLICANT'S INFORMATION DISCLOSURE STATEMENT	Atty. Docket No.: RPS920010172US1 (IRA-10-5709)	Serial No.: To be assigned
	Applicant: Atoji et al	
	Filing Date: Herewith	Group: To be assigned

U.S. PATENT DOCUMENTS

Initial*		Document No.	Date	Name	Class	Subcl.	Filing Date
	AA	5,815,688	09/29/1998	Averill	395	500	10/09/1996
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	AM	JP11232131A	02/13/1998	Japan			No
	AN	JP11230160A	01/16/1998	Japan			NO
	AO	JP10187475A	12/25/1996	Japan			No
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OTHER DOCUMENTS

	AR	"A Biased Random Instruction Generation Environment for Architectural Verification of Pipelined Processors", Journal of Electronic Testing: Theory and Applications, pgs. 13-27 (2000), Ta-Chung Chang
	AS	"Micro Architecture Coverage Directed Generation of Test Programs", Design Automation Conference, June 21-25, 1999, pgs. 175-180
	AT	"Verification by Behavorial Modeling – A Multiprocessor System Case, Conference on ASIC Proceedings", October 21-24, 1996, pgs 43-45
	AU	"Automatic Test Program Generation for Pipelined Processors", IEEE/ACM International Conference on CAD-94, November 6-10, 1994, pgs. 580-583

Examiner:	Date Considered:

*EXAMINER: Initial if reference considered, whether or not citation is in conformation with MPEP 609; draw line through citation if in conformance and not considered. Include copy of this form with next communication to applicant.